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The conventional operational amplifier parameters; design principles for MOST single bulk-driven amplifying stages

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Abstract:

This paper is devoted to study the principle of using the back-gate driven MOS principle will be used to design low-voltage low- power operation amplifiers, current mirrors, Fourth section describes the conventional operational amplifier parameters; it continues explaining design principles for MOST single bulk-driven amplifying stages, two stage bulk- driven, folded cascade bulk-driven and rail-to-rail bulk-driven op-amps in contrast to the conventional gate-driven technique to demonstrate its low voltage capability.

Keywords: op-amp, Bulk-driven op-amp, MOSTs, The Bulk-driven and Gate- Driven MOSFTs

الملخص:

تم تخصيص هذا البحث لدراسة مبدأ استخدام MOS الموجه بالبوابة الخلفية لتصميم مضخمات التشغيل ذات الجهد المنخفض والطاقة المنخفضة، وانعكاس التيار، ووصف معاملات مضخم التشغيل التقليدي؛ ويستمر في شرح مبادئ التصميم لمعظم مراحل التضخيم ذات البوابة الخلفية، والمضخمات التشغيلية ذات البوابتين الخلفيتين، وسلسلة متتالية ذات البوابة الخلفية، والمضخمات التشغيلية المدفوعة من الحاجز الي الحاجز على عكس التقنية التقليدية التي تعتمد على البوابة لإثبات انخفاضها قدرة الجهد.

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1.1 MOST: Single Bulk-Driven Amplifying Stages

An important factor concerning analog circuits is that the threshold voltages of future standard CMOS technologies are not expected to decrease much below what is available today. To overcome the threshold voltage a bulk-driven MOST has been used, it is well known that a reverse bias on the well-source junction will cause the threshold voltage to increase. [1,2,3,4,5] Similarly, a forward bias on this junction will cause the threshold voltage to decrease.

The bulk-driven transistor is a good solution to overcome the threshold voltage limitation. Because the bulk-driven transistor is a depletion type device, it can work under negative, zero, or even slightly positive biasing condition as depicted on Fig. 1.1

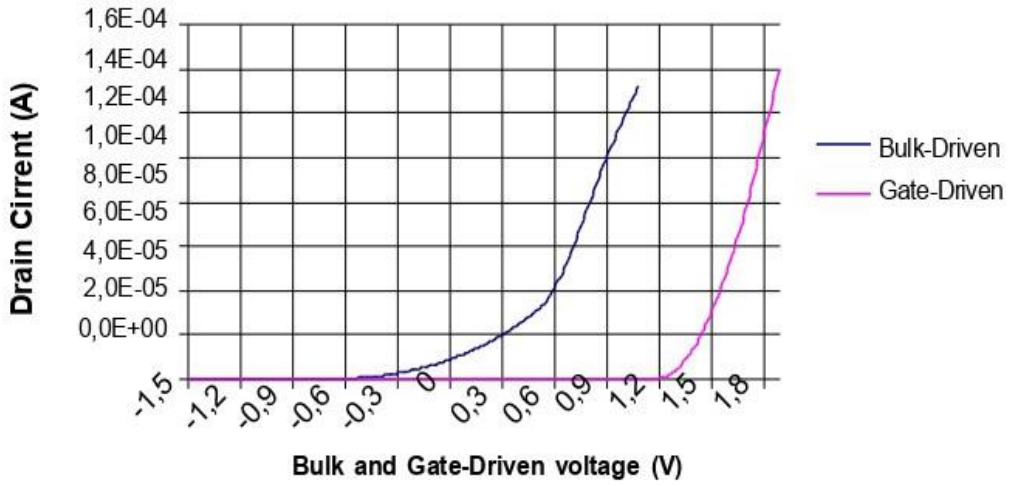

Figure 1.1 Drain current versus Bulk and Gate-Driven voltage

The operation of the bulk-driven MOST is much like a JFET. To enable bulk driving, one must first bias the gate to form a conduction channel inversion layer by connecting the gate terminal to a fixed voltage that is sufficient to form an inversion layer (e.g., $V_{GS} > V_T$ for the NMOS). By applying a potential difference between the drain and source, this inversion layer will act very much like a conduction channel of JFET (see Fig. 1.2). Since the bulk voltage affects the thickness of the depletion region associated with the inversion layer (conduction channel), the drain current can be modulated by varying the bulk voltage through the body effect of the MOST.

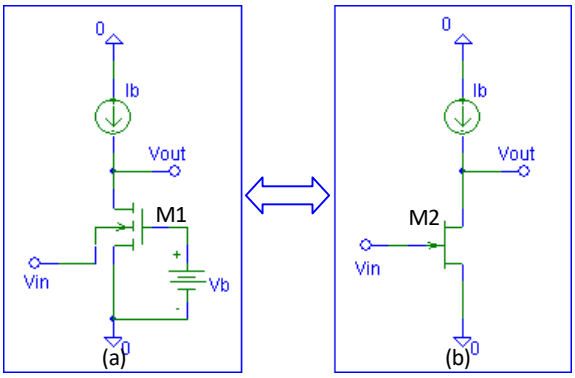

Figure 1.2 Bulk-driven MOS transistor (a), and its equivalent JFET (b).

The operation of the bulk-driven MOST is much like a JFET [6,7,8,9,10,]. To enable bulk driving, one must first bias the gate to form a conduction channel inversion layer by connecting the gate terminal to a fixed voltage that is sufficient to form an inversion layer (e.g., $V_{GS} > V_T$ for the NMOS). By applying a potential difference between the drain and source, this inversion layer will act very much like a conduction channel of JFET (see Fig. 1.3). Since the bulk voltage affects the thickness of the depletion region associated with the inversion layer (conduction channel), the drain current can be modulated by varying the bulk voltage through the body effect of the MOST.

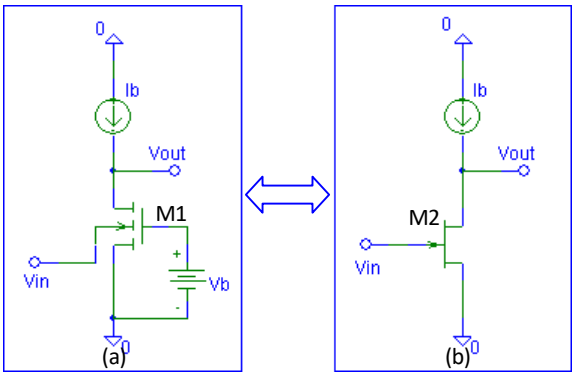

Figure 1.3 Bulk-driven MOS transistor (a), and its equivalent JFET (b).

For a MOST conductivity g_m is normally controlled by the gate capacitance. The voltage across the gate capacitance V_{GS} controls the conductivity of the channel. The drain current I_D of a MOST can also be controlled by bulk source voltage V_{BS}. The small signal equivalent circuit of Fig. 1.3 is depicted in the following figure.

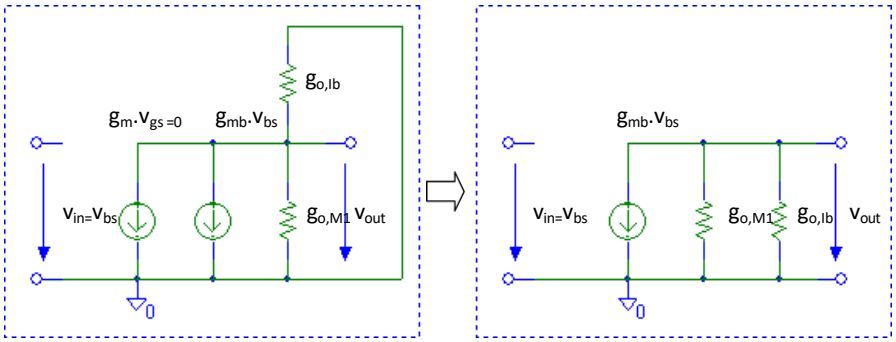

Figure 1.4 Small signal equivalent circuits

Actually, the g_{mb} is due to the existence of the bottom parasitic JFET (Fig. 1.3), which is formed by the channel and the bottom depletion layer capacitance. It can be utilized the parasitic JFET for signal processing purpose, if we apply signal to the bulk instead of to the gate and keep V_{GS} constant, then we have a bulk-driven MOS transistor. The gain of the bulk- driven op-amp is given by

$$A = \frac{V_{out}}{V_{in}} = \frac{g_{mb}}{g_{o,M1} + g_{o,Ib}} \qquad (4.1)$$

where $G_{m,eff} = g_{mb}$, and $g_{out} = g_{o,M1} + g_{o,Ib}$

Practically, V_{bs} should be less than the turn-on voltage of the bulk channel PN junction diode, $V_{bs} < V_{DIODE}$, where, V_{DIODE} is normally in the range of 0.6 to 0.7V.

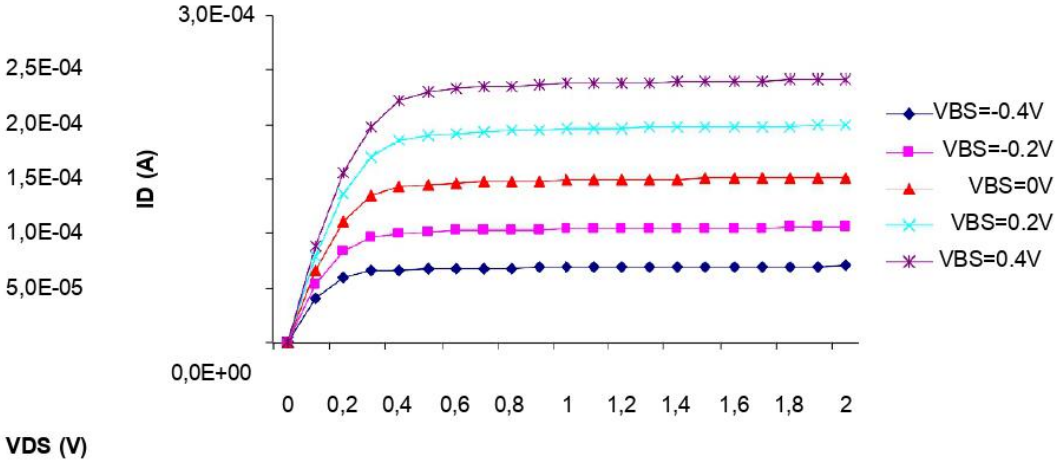

Figure 1.5 I-V static characteristic of the bulk-driven MOST for gate-source bias voltage 1V

Fig. 1.5 shows the I-V characteristic of the bulk-driven MOST for V_{GS}=1.2V and W/L=40µ/2µ. Increasing V_{BS}, V_{GS}, or W/L induces to increase the MOST drain current.

1.1 Two Stages Amplifier

In this part I will present a two stages bulk-driven amplifier that is able to run on low supply voltage.

A two-stage bulk-driven op-amp in CMOS is shown in Fig. 1.6. It consists of two stages, the first which is combined of the bulk-driven differential stage with pMOST input devices M_1 and M_2 and the current mirror M_3 and M_4 acting as an active load. The second stage is a simple CMOS inverter with M_7 as a driver and M_6 acting as an active load. Its output is connected to its input, i.e., to the output of the differential stage by means of compensation capacitance C_1 and resistance R_1. Since the compensation capacitance actually acts as a Miller capacitance in that stage,

Op-amp with bulk-driven input transistors has been designed. The design is depicted in the following figure.

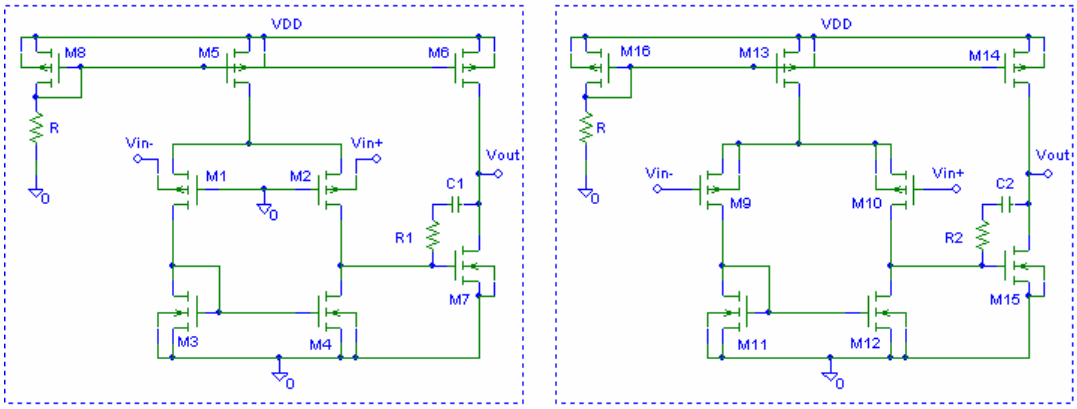

Figure 1.6 Bulk-driven op-amp (a) and conventional op-amp (b).

By setting the gate-source voltage to a value sufficient to tern on the transistor, then the operation of the bulk-driven MOST becomes a depletion type. Input voltage is applied to the bulk-terminal of the transistor to modulate the current flow through the transistor. The advantage of a bulk-driven device over a gate-driven device is that the threshold voltage limitation disappears and both positive and negative bias voltages (V_{BS}) are possible. This is especially important in analog low voltage circuits where the dynamic range of

the signal should be maximized with respect to the supply voltage in order to maximize the performance of the circuit.

There are also some drawbacks of bulk-driven devices compared to gate-driven devices, such as smaller transconductance (g_{mb} instead of g_m) because of smaller control capacitance of the depletion layer, larger parasitic capacitance to the substrate, which results in lower unity- gain frequency f_T, and higher input referred noise, because of smaller transconductance. Also, it has to be noted that a rail-to-rail bulk-driven op-amp need a twin-tub process. It should be mentioned that too much forward bias the bulk-source PN-junction, cause to appear the parasitic bipolar transistor effects like latch-up and/or excessive bulk and substrate-current.

The designed op-amp with bulk-driven input transistors is shown in Fig. 1.6. Because an N-well CMOS process has been used, the bulk-driven devices are of PMOS-type. By applying the input signal to the bulk-terminals instead of gate-terminals of the input transistors, the threshold voltage limitation disappears and a large input *CMR* of the op-amp is achievable. Another goal was to minimize current consumption and input referred noise. The noise at low frequencies is dominated by *1/f* noise. Choosing fairly large values for channel width and length of the input transistors M_1, M_2 and the channel length of the current mirror load transistors M_3, M_4, minimizes this noise. The large channel lengths in the input stage result in a large output impedance of the input stage, which increases the gain but decreases the bandwidth of the op-amp. The aspect ratio *W/L* of the input transistors is designed sufficiently large to limit the maximum possible negative V_{SB} to avoid large leakage currents from source to bulk and from source to substrate (in the case where the input voltage V_B is close to negative supply rail

Fig. 1.7 shows the simulation result of amplitude and phase frequency responses of the bulk-driven op-amp with a 1 V supply voltage. We can see that the bulk-driven technique removes the threshold voltage requirement of MOSTs from the signal path, and reducing the most serious limitation of analog MOST circuits as the power supply voltage.

The simulation results of the voltage bulk-driven are listed in Table 4.1.

Table 4.1 The simulation results of the open loop bulk-driven op-amp

Feature	Value	Unit
A_0	61	dB
Gain-bandwidth product	17	MHz
Offset	4	mV
Supply voltage	1	V
Input CMR	-0.25 to 0.3	V
Slew-rate	1.4	V/µs
Settling time	38	nsec
Load capacitance C_L	1	pF
Phase margin	76	Degree
Power consumption	31.3	µW

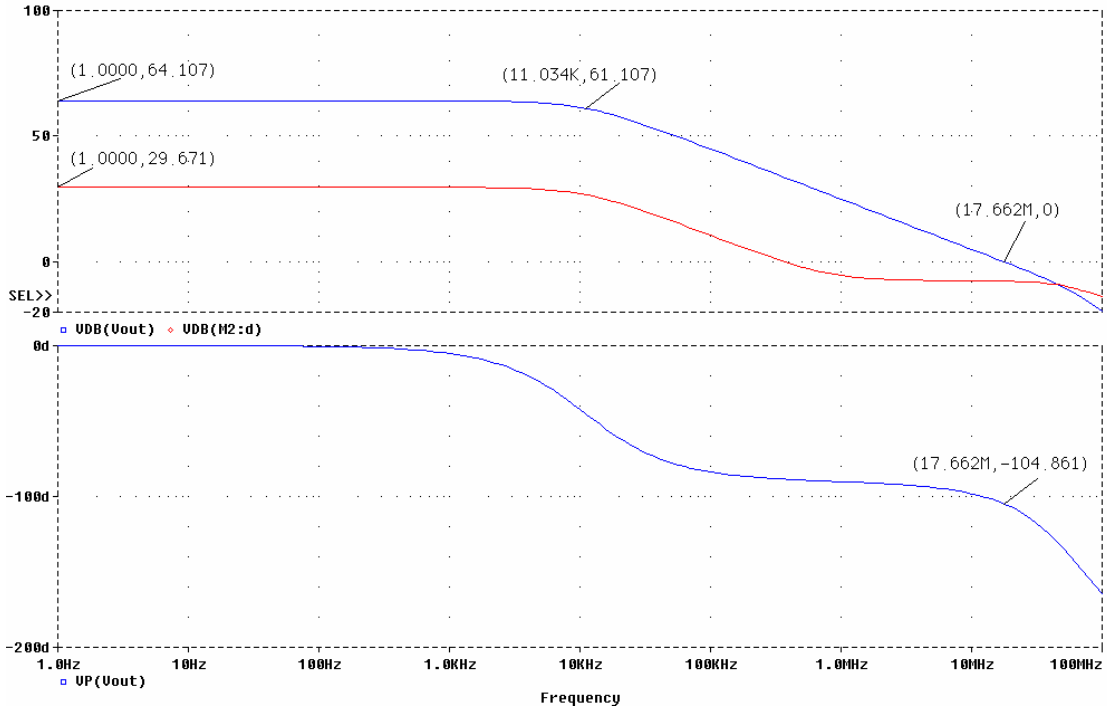

Figure 1.7 Amplitude and phase frequency responses of the bulk-driven op-amp.

1.1 Folded Cascade

To obtain a high output impedance in CMOS, a cascode stage could be placed straight on the input pair of the amplifier.

The folded-cascode amplifier is shown in Fig. 1.8. The name "folded-cascode" comes from folding down p-channel cascode active loads of a diff-pair and changing the MOSTs to n-channels. This amplifier, like all amplifier, has good PSRR compared to the two-stage amplifier since it is compensated with the load capacitance.

The folded cascode input stage, as shown in Fig. 1.8 increase the common-mode input voltage range, since we replace a current source M7-M8 instead of a current mirror which its used typically in the conventional op-amp.

The input stages consist of a N-channel bulk-driven differential pair M1-M2, folded cascodes M9-M10, providing a level shift function, and a bulk-driven current mirror M11-M14, providing a differential to single ended convention. The transistors M7-M8 function as bias current source. In order to maximize the output current of the input stage, these current sources are biased at the same value as the tail current source of M3-M4.

Since the output resistance is one of the most important performance parameters for a current mirror, and the value of this resistance is almost equal for both gate-driven and bulk- driven current mirrors, that's way it was used the bulk-driven folded cascode current M3-M4 biased by M5-M6, this type of connection is suitable for low voltage applications.

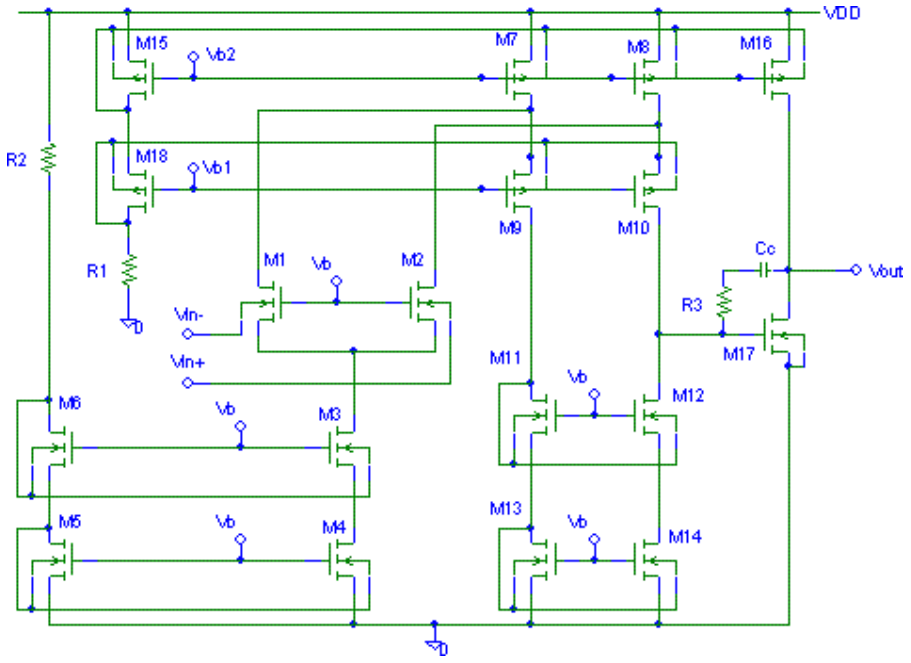

Figure 1.8 Folded-cascode bulk-driven op-amp.

The drain voltage of both input transistor can reach the positive supply voltage within one saturation voltage of the current source M_7-M_8. This saturation voltage is, generally, much smaller than a gate source voltage.

2. Conclusions

describes the conventional operational amplifier parameters; it continues explaining design principles for MOST single bulk-driven amplifying stages, two stage bulk- driven, folded cascode bulk-driven and rail-to-rail bulk-driven op-amps in contrast to the conventional gate-driven technique to demonstrate its low voltage capability.

I had verified the principle of the bulk-driven MOS transistor as a differential stage amplifier, and then I started applying this principle to achieve a completely novel family of amplifiers, two stages bulk-driven amplifier, folded cascode bulk-driven amplifier and finally rail-to-rail bulk-driven amplifier. Low-voltage capability of those bulk- driven function blocks has been assured in contrast to its function identical gate-driven MOST.

Based on the results I had achieved I could present the main advantages and disadvantages of bulk-driven technique.

- The polarity of the bulk-driven MOST is technology related. For a P (N) well CMOS process, only N (P) channel bulk-driven MOSTs are available. This may limit its applications. For example a rail-to-rail bulk-driven op-amp needs a dual well process to realize it.
- The equivalent input referred noise of a bulk-driven MOS amplifier is larger than a conventional gate-driven MOS amplifier because of its smaller transconductance.
- Prone to turn on the bulk-channel PN junction, which may result in a latch-up problem.
- Rail-to-rail op-amp need separate wells (dual well process), which is:

- More expensive process
- Bigger chip area needed
- Worst matching comparing with one well process

- The bulk-driven circuits could have a role to play in many applications, which needs low-voltage low-power current mirrors, current sources, and conventional op-amp applications ranging from unity-gain buffer, signal amplifiers, to filters and switched capacitor, and so on.

- With respect to above mentioned discussions it is declared that aims of this thesis were fulfilled.

1. Margins:

2. MD Hasanuzzaman, Sred K. Islam, Leon M. Tolbert, Burak Ozpineci: "Design, Modelling , Testing and Spice Parameter Extracting of Transistor in 4H-Silicon Carbide", Frontiers in Electronics, pp. 733.-746.,2005.
3. A. Elasser and T.P. Chow, "Silicon Carbide Benefits and Advantages for Power Electronics Circuits and Systems," Proc. IEEE, 2002: 90(6): 969-86.
4. Zau J., D kotchetkov and AA Balankin "Thermal conductivity of GaN films: Effects of impurities and dislocations" Journal of Applied Physics 92, (2002) p.2534
5. A. Power and L. Rowland: "SiC Materials- Progress, Status and Potential Roadblocks, Processing IEEE, pp.942.-955.,90(6).2002.
6. J .R. Brews, A charge sheet model of the MOSFET, Solid State Electron. 21 (1978) 345–355.
7. M . Roschke, F. Schwierz, Electron mobility model for 4H, 6H and 3C SiC, IEEE Trans. Electron Dev. 48 (2001) 1442–1447.
8. Hasanuzzaman M, Islam SK, Tolbert LM, Ozpineci B. Model simulation and verification of a vertical double implanted (DIMOS) transistor in 4H-SiC, In: Proc the IASTED International Conference on Power System Palm Spring 2003 p. 313–6.
9. Nakashima and H.Harima, "Characterization of structural and electrical properties in SiC by Raman spectroscopy", in Inst. Phys. Conf. Series, p. 269,(1969).
10. T. Kinoshita, K. Muto, M. Schadt, G. Pensl, and K. Takeda,"Calculation of the anisotropy of the Hall mobility in N-type 4H- and 6H-SiC", Mat. Sci. Forum, vols.264-268,p.295,1998.
11. M. Schadt, G. Pensl. R . P. Devaty, W, J , Choyke, R. Stein. And D. Stephany, "Anisortropy of the electron Hall in 4H,6H, Choyke, and 15R silicon carbide", Appl. Phys. Lett, vol. 65, p. 3120.1994.
12. Krishna Shenai, Effect of P-Base sheet and contact Resistances on Static current-voltage Characteristics of Scaled low-voltage Vertical Power DMOSFETs, IEEE Electron Devices Letters, no. 6, pp. 270-272,1991.

References:

13. A. Elasser and T.P. Chow, "Silicon Carbide Benefits and Advantages for Power Electronics Circuits and Systems," Proc. IEEE.
14. A. Power and L. Rowland: "SiC Materials- Progress, Status and Potential Roadblocks, Processing IEEE.
15. Hasanuzzaman M, Islam SK, Tolbert LM, Ozpineci B. Model simulation and verification of a vertical double implanted (DIMOS) transistor in 4H-SiC, In: Proc the IASTED International Conference on Power System Palm Spring.
16. J .R. Brews, A charge sheet model of the MOSFET, Solid State Electron.
17. Krishna Shenai, Effect of P-Base sheet and contact Resistances on Static current-voltage Characteristics of Scaled low-voltage Vertical Power DMOSFETs, IEEE Electron Devices Letters.
18. M . Roschke, F. Schwierz, Electron mobility model for 4H, 6H and 3C SiC, IEEE Trans. Electron Dev.
19. M. Schadt, G. Pensl. R . P. Devaty, W, J , Choyke, R. Stein. And D. Stephany, "Anisortropy of the electron Hall in 4H,6H, Choyke, and 15R silicon carbide", Appl. Phys.
20. MD Hasanuzzaman, Sred K. Islam, Leon M. Tolbert, Burak Ozpineci: "Design, Modelling , Testing and Spice Parameter Extracting of Transistor in 4H-Silicon Carbide", Frontiers in Electronics, pp.
21. Nakashima and H.Harima, "Characterization of structural and electrical properties in SiC by Raman spectroscopy", in Inst. Phys. Conf. Series.
22. T. Kinoshita, K. Muto, M. Schadt, G. Pensl, and K. Takeda,"Calculation of the anisotropy of the Hall mobility in N-type 4H- and 6H-SiC", Mat. Sci. Forum.
23. Zau J., D kotchetkov and AA Balankin “Thermal conductivity of GaN films: Effects of impurities and dislocations” Journal of Applied Physics .